CLAIMS

Now, therefore, the following is claimed:

1. A computer system for processing instructions of a computer program, comprising:

a plurality of pipelines configured to process and execute said instructions; and

a scoreboard coupled to said pipeline, said scoreboard having a plurality of multi-bit registers, said scoreboard configured to receive a register identifier from one of said pipelines and to change a first bit in one of said multi-bit registers in response to said register identifier, said first bit indicating whether a pending write to a register identified by said register identifier exists, said register identifier associated with one of said instructions processed by said pipeline, said scoreboard further configured to receive data associated with said one instruction and to change a second bit in said one register based on said received data.

2, The system of claim 1, wherein said data associated with said one instruction includes a speculative bit.

3. The system of claim 1, wherein said one instruction is a load instruction and said data associated with said one instruction is indicative of which memory locations have been searched in response to said one instruction.

4. The system of claim 3, further comprising circuitry configured to detect whether said one instruction can be canceled based on said second bit.

5. The system of claim 1, further comprising circuitry coupled to said scoreboard, said circuitry configured to detect a data hazard based on said first and second bits.

6. The system of claim 5, wherein said second bit indicates whether said one instruction is speculative, said circuitry further configured to detect whether another instruction being processed by one of said pipelines utilizes said register identified by said register identifier and to modify said second bit in response to said other instruction.

7. The system of claim 5, wherein said circuitry is further configured to modify said second bit.

8. A method for processing instructions of a computer program, comprising the steps of:

providing a pipeline and a scoreboard, said scoreboard including a plurality of multi-bit registers;

processing one of said instructions via said pipeline;

transmitting a register identifier defined by said one instruction to said scoreboard;

changing a first bit in one of said multi-bit registers based on said register identifier;

transmitting data associated with said one instruction to said scoreboard;

changing a second bit in said one register based on said data; and

detecting that data produced via execution of said one instruction is unavailable; and

performing said changing a first bit step in response to said step of detecting that data produced via execution of said one instruction is unavailable.

9. The method of claim 8, further comprising the step of detecting a data hazard based on said first and second bits.

10. The method of claim 8, further comprising the step of indicating, via said second bit, a speculative state of said one instruction.

11. The method of claim 8, further comprising the steps of:

detecting whether another instruction, when executed, utilizes a register identified by said register identifier; and

changing said second bit based on said detecting whether another instruction utilizes said register step.

12. The method of claim 8, further comprising the steps of:

retiring said one instruction; and

performing said changing a first bit step in response to said retiring step.

13. The method of claim 8, wherein said processing step further includes the step of executing said one instruction and said method further includes the steps of:

receiving data produced in response to said executing step; and

changing said first bit in response to said receiving step.

14. The method of claim 8, further comprising the steps of:

retrieving data in response to said one instruction; and

indicating, via said second bit, how far said retrieving step has progressed.

15. The method of claim 14, further comprising the steps of:

detecting whether said one instruction can be canceled based on said second bit; and

canceling said one instruction based on said detecting whether said one instruction can be canceled step.

16. The method of claim 8, further comprising the steps of:

selecting said one register based on said register identifier; and

performing said changing a first bit step in response to said selecting step.

17. The method of claim 16, further comprising the step of:

performing said changing a second bit step in response to said selecting step.

18. A method for processing instructions of a computer program, comprising the steps of:

providing at least one pipeline and a scoreboard, said scoreboard including at least one multi-bit register;

processing at least one instruction via said one pipeline;

identifying a register based on a register identifier defined by said one instruction;

detecting whether data produced via execution of said one instruction has been written to said register identified in said identifying step;

transmitting said register identifier to said scoreboard in response to a detection in said detecting step that said data produced via execution of said one instruction has yet to be written to said register identified in said identifying step;

changing a first bit in said one register based on said register identifier transmitted in said transmitting said register identifier step;

receiving, at said scoreboard, data associated with said one instruction;

changing a second bit in said one register based on said data received in said receiving step; and

detecting a data hazard based on said first and second bits.

19. The method of claim 18, further comprising the steps of:

retiring said one instruction; and

performing said changing a first bit step in response to said retiring step.